

# ON CHIP TIMING ADJUSTMENT IN MULTI-CHANNEL FAST DATA TRANSFER

## Abstract of the Disclosure

A method and structure for an apparatus for maintaining signal integrity between integrated circuits residing on a printed circuit board. The apparatus has adjustable delay circuitry within the circuits and the adjustable delay circuitry adjusts the timing of signals processed within the circuit. A phase monitor connects to the circuits. The phase monitor detects phase differences between signals output by the circuits. A controller connected to the delay circuitry, the phase monitor, and the controller adjust the delay circuitry to compensate for the phase differences.

## Figures

Figure 1: A line graph showing the relationship between the number of hours spent studying and the score on a test. The x-axis represents 'Hours Studied' (0 to 10) and the y-axis represents 'Test Score' (0 to 100). The data points are as follows:

Hours Studied	Test Score
0	50
1	55
2	60
3	65
4	70
5	75
6	80
7	85
8	90
9	95
10	100